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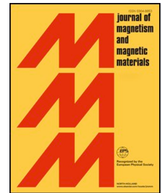
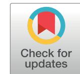


Comprehensive study of spin field effect transistors with co-graphene ferromagnetic contacts



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ABSTRACT

Two-dimensional graphene is considered potent candidate for the development of spintronics technology. Present work reports study of graphene-based spin-Field Effect Transistors.

(s-FET) of two types namely, Top-Gated s-FET and Back-Gated s-FET. The Ohmic contact behavior was analyzed as Co-Graphene nanosheets (CGNs) used as ferromagnetic electrode for both types of s-FETs. The magnetoresistance (MR) study is conducted for both devices as a function of temperature and gate voltage. Study shows that MR monotonically reduces as temperature increases. For greater insight into about the functioning of device, spin-polarization values were estimated at different temperatures. Switching action in both the devices was analyzed and finally it is found that Top-Gated Type s-FET shows appropriate switching action.

1. Introduction

Spin-field effect transistor (s-FET) is the new type of electronic device, which comes with additional feature of spin-based magnetoresistance. In s-FET, switching action can be achieved by spin precession or dephasing of spin-polarized carriers injected into the channel. The concept of s-FET was first time coined by Datta and Das [1]. After this wide range of s-FETs were proposed by many researchers on the basis of their operating principles [2,3]. In semiconductor spintronics, various phenomenon such as spin–orbit interaction, coupling of electron spin to external electric fields, spin transport through semiconductor channel with spin–orbit coupling and spin-Hall effect plays very crucial role [4]. By employing magnetic field and controlling gate bias, the parallel and antiparallel spin-state of electron and subsequently magnetization of the ferromagnetic contacts can be achieved. In this way, output currents depend on spin-state of electron and magnetization. The high current state is associated with parallel spin state of electron, however low current is associated with anti- parallel spin state [5,6].

For s-FET operation, three major conditions must be satisfied. First requirement is the injection of spin-polarized electrons from ferromagnetic source into 2-dimensional electron gas channel. Second requirement is the transport of electrons through 2-dimensional electron gas channel without losing spin state. Third requirement is the detection of spin-state electron by ferromagnetic drain [7]. Besides these requirements, two main challenges are associated with s-FET, first is the leakage current in the off-state and second is the spin relaxation in the channel. But these issues can be resolved by two approaches, by choosing materials with a long spin de-phasing length and strong spin–orbit coupling [8].

The performance of s-FET is also affected by conductivity mismatch problem between ferromagnetic electrode and semiconductor channel. To resolve the issue of conductivity mismatch, few reports suggested that the use of graphene as tunnel barrier is appropriate option, because the significant lateral transport and low out of-plane conductivity of graphene [9–12].

Another reason for graphene appropriateness for spintronics application is that it has unique characteristics related to spin-polarized electrons. The spin-polarized electron in graphene can travel tens of microns without losing spin orientation at room temperature. This characteristic of graphene makes it enable for long-distance spin communication in future spintronic technologies [13–15].

In the present study, Cobalt-Graphene nanosheets are chosen as ferromagnetic material for source and drain contacts due to long spin relaxation distances of graphene than any other traditional metals and semiconductors [16–18]. In addition to this, another feature of graphene is that, it can conduct spin current up to macroscopic distances due to weak spin-orbit and hyperfine couplings in carbon materials [19].

Here, two types of s-FET namely Top-Gated s-FET and Back-Gated s-FET are reported. In this study, Co-Graphene nanosheets (CGNs) were

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used as ferromagnetic contact for source and drain purpose. The Ohmic nature of contacts are also discussed in this work. The magnetoresistance curves were recorded as the function of temperature and gate voltage. Switching action for both the types of devices is also studied.

2. Experimentation

2.1. Preparation of Co-Graphene nanosheets

The necessary amount of Co-Graphene nanosheets (CGNs) were prepared by ex-situ approach. The graphene for preparation was obtained by using previously reported method [20]. To prepare the CGNs, 10 g of graphene sheets were dissolved in 50 ml acetic acid under rigorous magnetic stirring for 30 min. After magnetic stirring, solution was kept under probe-sonication for 1 h. During this step, separate solution of 0.5 g of $Co(NO_3)_3$ was dissolved in 10 ml of acetic acid and kept for 30 min under magnetic stirring. This solution was added in former solution in drop-wise manner under constant magnetic stirring. Final solution was then filtered and washed several times by deionized water. The black colored precipitate was collected and dried at 100 °C in oven.

To form homogeneous magnetic system, CGNs were kept for heating in the temperature range of 100 to 500 °C in stepwise manner with an interval of 100 °C. At each temperature value, sample was heated for 60 min. Similarly, the sample was allowed to cool at 400, 300, 200 and 100 °C each for 60 min.

2.2. Materials characterization techniques

The structural study of CGNs was completed using X-ray diffraction (XRD) technique (Rigaku Miniflex-XRD; Wavelength = 1.5406 Å). The surface study of CGNs was performed by field emission scanning electron microscopy (FESEM) on SEM instrument, Model: ZEISS SIGMA operating at 5 kV ETH voltage. The elemental analysis was done using an energy dispersive X-ray analysis (EDAX) instrument, Model: EAG AN461. The magnetic behavior of CGNs was studied using Vibrating Sample Magnetometer technique (Quantum Design Model- PAR 155) having specifications as Range: 0.00001 to 10,000 emu and Magnetic field: −10 to +10 kOe.

2.3. Device fabrication and measurements

2.3.1. Top-Gated s-FET

For the fabrication of Top-Gated s-FET, required heavily doped n-type silicon wafer was procured from India-Mart of thickness 500 µm. Before starting the device fabrication process, n-type silicon wafer was kept for cleaning process to break the bonds between substrate and contaminants present on substrate in the form of grease, adsorbed water molecule and air borne dust.

In the cleaning process of substrate, firstly the substrate was washed with mild-detergent solution (Labolene) and then with distilled water. Subsequent to this step, substrate was kept in NaOH solution for the removal of acidic contaminations and then again washed with distilled water. Finally, the substrate was kept in alcohol vapors. After completion of cleaning process, the substrate was kept for etching to pattern Co-Graphene based ferromagnetic electrodes. In this process, buffered hydrofluoric acid was used as etchants. The remaining area of substrate was masked with kapton tape. The Co-Graphene based ferromagnetic material was used as source and drain contacts on substrate.

The electrode material that is Co-Graphene and gate were deposited by using photolithography technique. The electrode material Co-Graphene was achieved by depositing cobalt on previously deposited graphene. After deposition of FM contacts as source and drain, polyvinyl acetate was deposited on the channel between FM electrodes using spin-coating technique. The fabricated device has channel length of the order of 1.21 µm and channel width 14.25 µm. Fig. 1(a) depicts the schematic drawing of Top-Gated s-FET structure and Fig. 1(b) shows the scanning electron micrograph of s-FET, with all necessary components displayed on SEM image with circuitry arrangement.

2.3.2. Back Gated s-FET

All necessary components required for the s-FET fabrication procured from India-Mart. Before the fabrication of device, substrate was cleaned according to the process discussed in the earlier section. To fabricate the back-gate configuration type s-FET [21], the heavily doped n-type silicon having 1 µm thick thermally oxidized SiO_2 layer on the surface was used as the substrate. For the formation of 2-dimensional electron gas condition, heavily doped n-type semiconducting layer was fixed on thermally oxidized SiO_2 layer. The thermally oxidized SiO_2 layer of substrate was used as gate insulator, whereas the heavily doped n-type silicon part of substrate was used as gate electrode. The Co-Graphene based ferromagnetic electrodes as source and drain were designed on 2-dimensional electron gas layer by photolithography. The fabricated device has channel length of the order 1.2 µm and channel width 12.1 µm. Fig. 2(a) depicts the schematic drawing of back-gated type s-FET structure and Fig. 2(b) shows the scanning electron micrograph of s-FET, with all necessary components of s-FET displayed on SEM image with circuitry arrangement.

2.3.3. Device characterization and measurements

The transport measurements for Top-Gated s-FET and Back-Gated s-FET were performed using Physical Properties Measurements System (PPMS) made by Quantum Design.

The Ohmic contact characteristics of devices were studied using current-voltage (IV) curves. The performance of s-FET was analyzed by measuring the electrical resistance as a function of magnetic field. It is well known that electrical resistance can be tuned into the high and low-resistance state by sweeping the magnetic field.

Magnetoresistance (MR) is defined as, $MR\% = [(R_{ap} - R_p)/R_p] \times 100$, where R_{ap} is magnetization vectors of two electrodes are antiparallel and R_p is the magnetization vectors of two electrodes are parallel. MR curves were recorded for different values of temperature and gate voltage.

3. Results and discussion

3.1. XRD, SEM and VSM study

Fig. 3(a) shows the XRD pattern of CGNs, comprised of two broad peaks at 26.3° and 44.2° with Miller indices (0 0 2) and (1 0 0), respectively. These peaks are signature peaks of graphene [22]. No separate peak was obtained for Co, which indicates that the orientation of graphene layers is unchanged. Fig. 3(b) depicts the SEM images and elemental X-ray mapping of CGNs. The SEM image confirmed that Co nanocrystals are uniformly spread on graphene surface and elemental analysis also confirmed that Co nanocrystals are distributed over the graphene surface. Actually, the pure graphene is a diamagnetic material due to sp^2 hybridization. The graphene used in this study was synthesized using electrochemical exfoliation of graphite, which certainly contains defects, which imprint magnetic features into graphene [23]. Many reports demonstrated that magnetic properties can be instilled in graphene, by adding ferromagnetic metal in graphene [24–26]. In present study, magnetic properties imprinted in graphene by decorating its surface with Co particles. Fig. 3(c) shows the hysteresis loops of CGNs recorded at room temperature (298 K). The good quality hysteresis loops of CGNs indicates that prepared CGNs comprises of good ferromagnetic ordering. The values of coercivity, remanant magnetization and saturation magnetization estimated from hysteresis loop were 537 Gauss, 0.2002 emu/gm and 0.761 emu/g, respectively. It shows that Co-graphene system comprise the ferromagnetic-like behavior, which characteristically correlate with the existence of interaction between graphene and Co Also, electronic structure modifications and

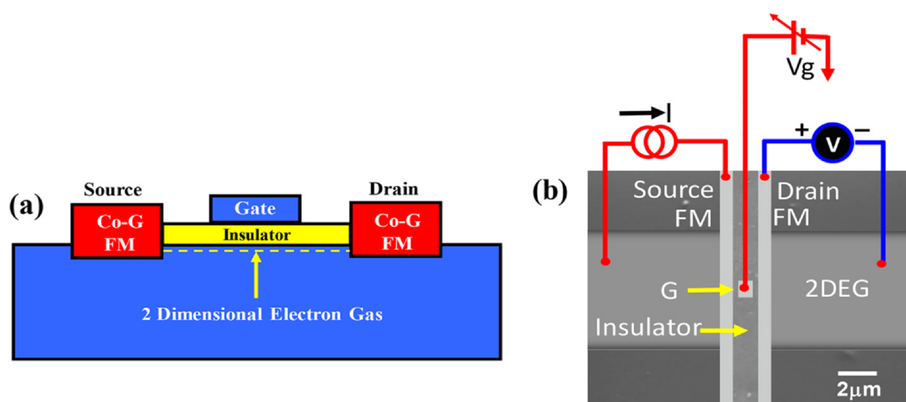

Fig. 1. (a) Schematic drawing of Top-Gated s-FET structure and (b) Scanning electron micrograph of s-FET. For better understanding, all necessary components of s-FET are displayed on SEM image with circuitry arrangement.

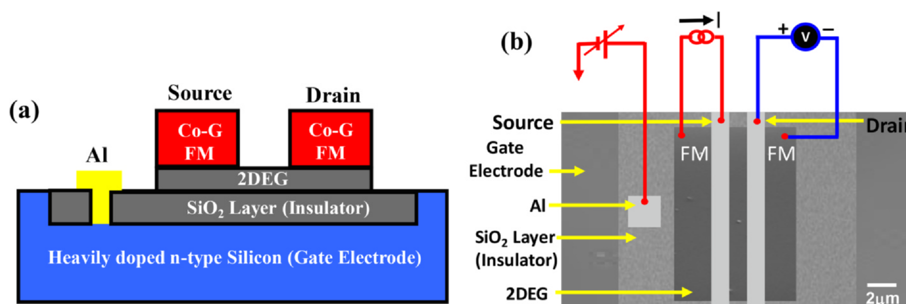

Fig. 2. (a) Schematic drawing of Back-Gated Type s-FET structure and (b) Scanning electron micrograph of s-FET. For better understanding, all necessary components of s-FET were displayed on SEM image with circuitry arrangement.

symmetry breaking in Co-graphene system improves the magnetic properties of system [27].

Fig. 3(d) shows the magnetoconductance curve of CGNs as a function of the magnetic field at different temperatures. The magnetoconductance in CGNs is attributed to weak spin-orbit coupling. Magnetoconductance gives insight to study microscopic behavior of ferromagnetic materials. This parameter also helps to identify scattering centers in ferromagnetic materials [28]. The positive value of magnetoconductance was obtained on entire scale of magnetic field for all temperatures. Similarly, the magnetoresistance curve did not exhibit

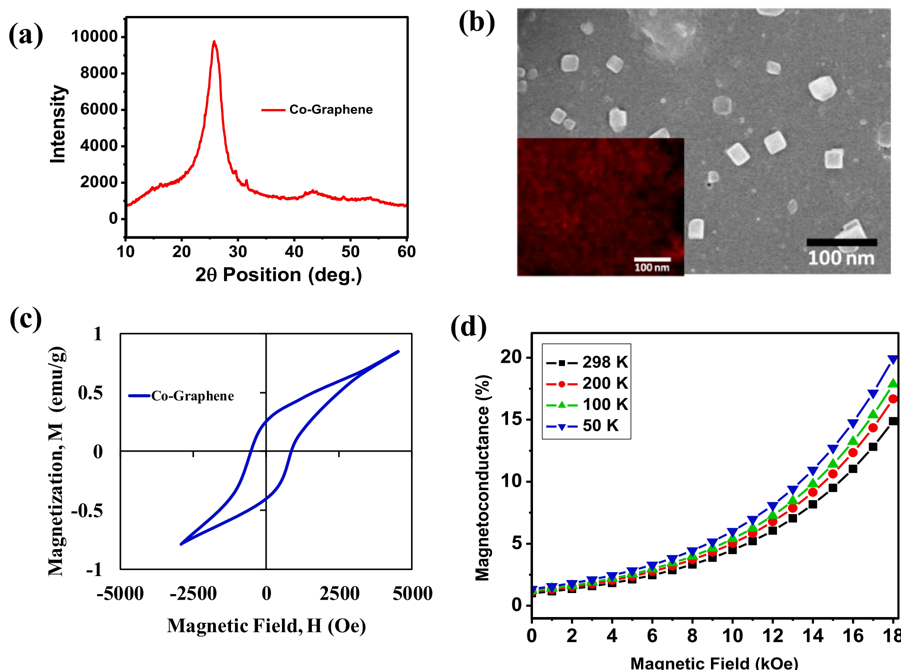

Fig. 3. (a) XRD pattern, (b) SEM images with elemental X-ray mapping of elements (inset), (c) VSM hysteresis loop and (d) Magnetoconductance as a function of magnetic field at different temperature of CGNs.

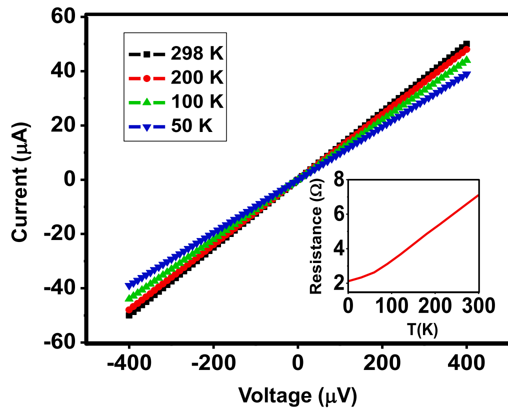

Fig. 4. Current-voltage curves of device at different temperature and inset shows variation of resistance curve with temperature at zero magnetic field.

any peak in low magnetic field. This indicates intrinsic impurities or defects have negligible contribution in magnetoconductance [29]. The magnetoconductance curve with no peak reflects that good quality interfaces formed between graphene and cobalt.

3.2. Ohmic contact study

Fig. 4 displays the current-voltage (I-V) curves of the device recorded at different temperatures (50, 100, 200 and 298 K) to study the behavior of contacts between CGNs and 2-dimensional electron gas. The linear nature of curve indicates that contact used in fabrication of Top-Gated s-FET device has Ohmic nature. Inset of Fig. 4 shows that the resistance increases with increasing temperature, indicates that 2-dimensional electron gas in device behaves like metal. The behavior of curve also suggests that 2-dimensional electron gas channel works like conducting thin film between two CGNs based FM electrodes [30]. The results obtained for Ohmic study have good agreement with other reports in literature. The researcher's team of Samsung Advanced Institute of Technology studied critically the effect of graphene insertion on the behavior of Ohmic contacts in metal-semiconductor. This work concluded that metal deposited graphene has reduced the work

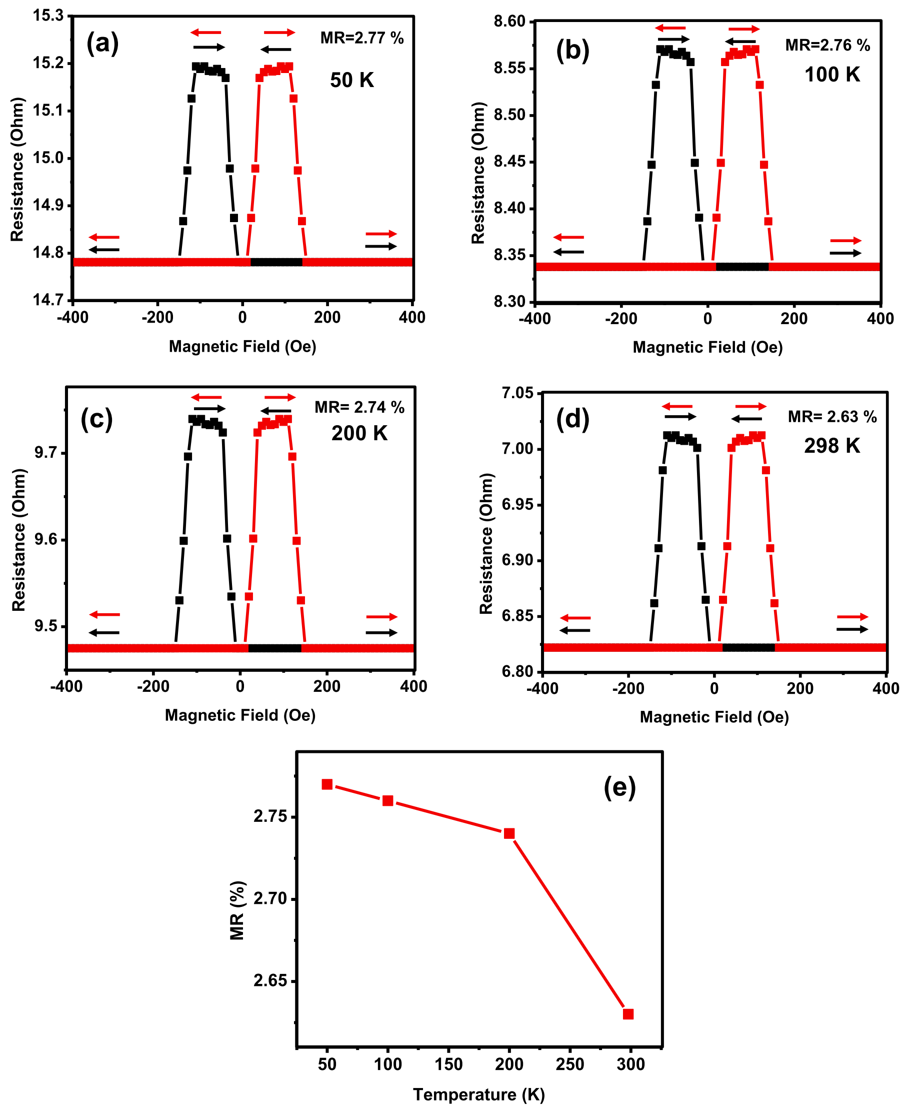

Fig. 5. Magnetoresistance ratio of device (Top-Gated s-FET) as a function of magnetic field at temperature (a) 50 K, (b) 100 K, (c) 200 K and (d) 298 K. Magnetoresistance ratio is high for the antiparallel magnetization configuration and low for parallel magnetization configuration. (e) Variation of magnetoresistance ratio with temperature.

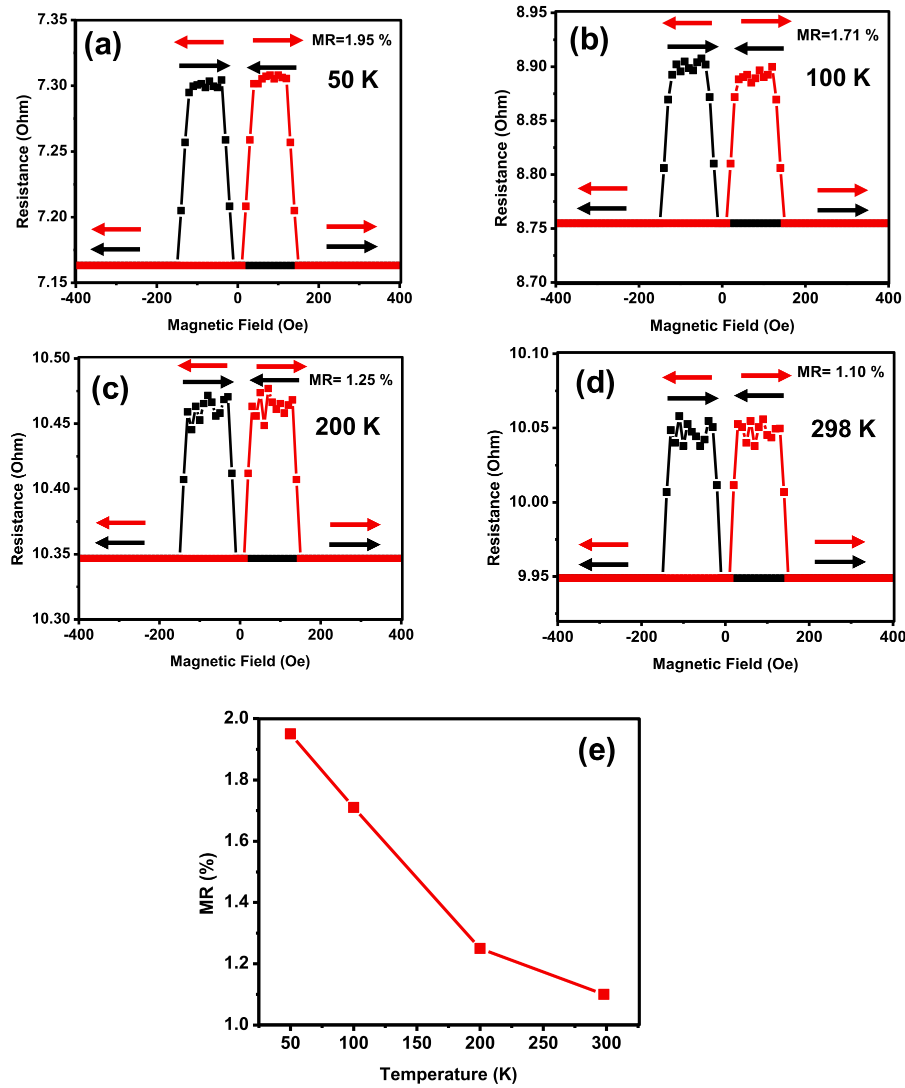

Fig. 6. Magnetoresistance ratio of device (Back-Gated s-FET) as a function of magnetic field at temperature (a) 50 K, (b) 100 K, (c) 200 K and (d) 298 K. (e) Variation of magnetoresistance ratio with temperature.

Table 1
MR and spin-polarization values of CGNs based ferromagnetic electrodes used for fabrication of Top-Gated s-FET and Back-Gated s-FET.

Temperature (K)	MR %	Amplitude of MR curve (Ω)	Spin-Polarization
Top-Gated s-FET			
50	2.77	0.42	0.374
100	2.76	0.23	0.276
200	2.74	0.26	0.294
298	2.63	0.18	0.244
Back-Gated s-FET			
50	1.95	0.14	0.216
100	1.71	0.15	0.223
200	1.25	0.13	0.208
298	1.10	0.11	0.191

function of graphene. In other words, it reduces the height of Schottky barrier at the metal-semiconductor junction [31]. Another report on graphene based Ohmic contact at metal–semiconductor junctions supports that insertion of graphene between metal-semiconductor reduces the Schottky barrier height and enhances the Ohmic characteristics [32].

3.3. Variation of magnetoresistance with temperature

Fig. 5(a–d) shows a series of MR curves for Top-Gated s-FET at different temperatures ranging from 50 K to 298 K. The highest value of MR% was found to be 2.77% at 50 K. Fig. 5(e) shows the variation of MR% with temperature. Similarly, Fig. 6(a–d) shows the MR curves for Back-Gated s-FET recorded at different temperatures ranging from 50 K to 298 K. For Back Gated s-FET, the highest value of MR% was found to be 1.95% at 50 K. Fig. 6(e) shows the variation of MR% with temperature.

In both type of s-FETs, magnitude of the MR monotonically decreases as the temperature increases. This behavior of MR curve attributed to inelastic scattering with phonons, surface states, and thermal smearing of energy distribution in the ferromagnetic material [33,34].

Whereas the highest value of MR for both devices at 50 K, attributed to the higher value of spin-polarization. For Top-Gated s-FET, the value of spin-polarization was found to be 0.374 and for Back-Gated s-FET, its value was 0.216. This study also discloses that spin-polarization in ferromagnetic materials reduces by increasing temperature.

In spintronics technology, spin polarization of ferromagnetic material plays a very crucial role. Because, ferromagnetic materials are the ideal foundation for spin polarized carriers because of their intrinsic

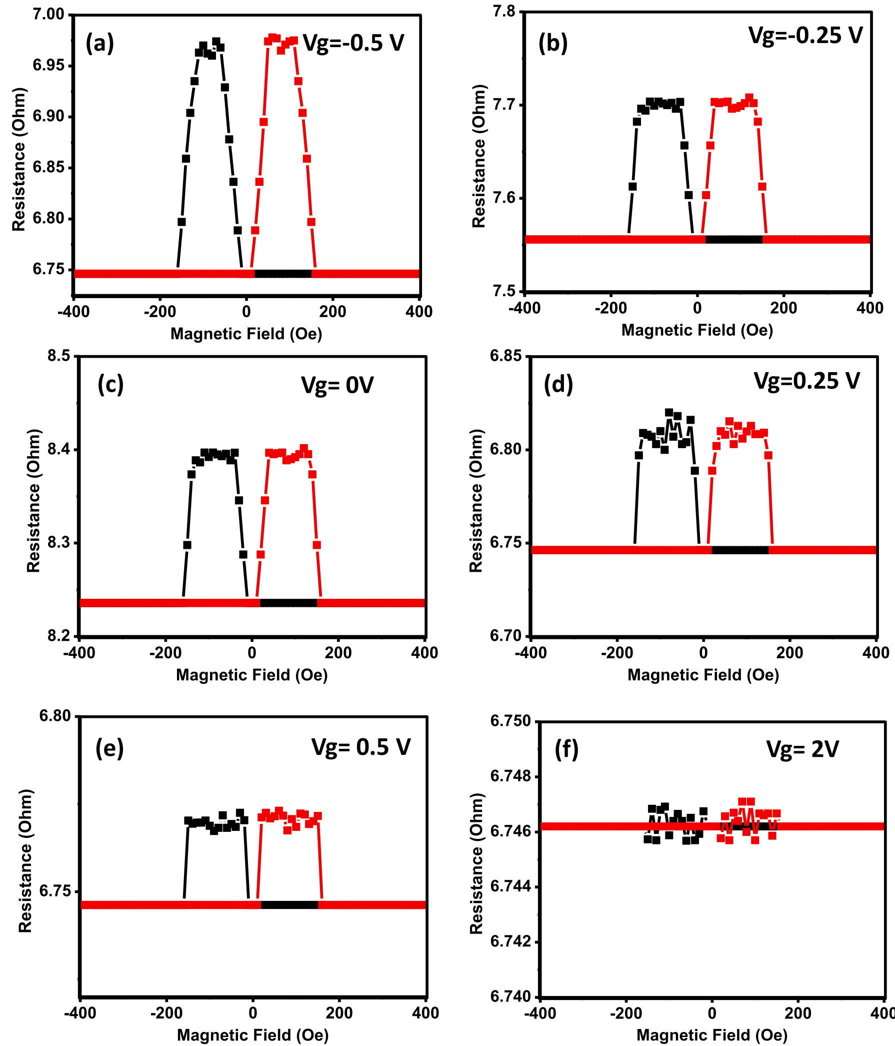

Fig. 7. Gate-controlled MR measurements in Top-Gated s-FET at gate voltage (a) −0.5 V, (b) 0.25 V, (c) 0 V, (d) 0.25 V, (e) 0.5 V and (f) 2 V at room temperature 298 K.

spin polarization. Ferromagnetic materials have an imbalance among the number of charges having particular spin orientation at the Fermi level. This imbalance in spin orientation at the Fermi level results in net spin polarization of the conduction electrons. The spin polarization P of a material is defined by (Eq. (1)),

$$P = \frac{n_\uparrow - n_\downarrow}{n_\uparrow + n_\downarrow} \tag{1}$$

where, n↑ and n↓ are spin orientation of charges in material.

The relation between the MR and polarization of ferromagnetic electrode can be approximated as (Eq. (2)),

$$MR = \frac{2P_1P_2e^{\frac{-d}{\lambda S}}}{1 - P_1P_2e^{\frac{-d}{\lambda S}}} \tag{2}$$

where d is the length of the trajectories of the electrons. λs is spin diffusion length. Assuming efficient spin transport, we could say surviving probability factor $[\exp(-d/\lambda_s)] \sim 1$.

In the present study, both contacts materials that is CGNs based FM electrodes have been used, hence their spin-polarization value is assumed as same (P1 ≈ P2 = P). Thus, by using Eqs. (1) and (2), the spin-polarization values at different temperatures were estimated as listed in Table 1. To the best of our knowledge, this is one of the first reports which speaks about the spin-polarization of Co-graphene system for spin-field effect transistor application. Dayen et al recently published detailed report on two-dimensional van der Waals spin-interfaces and magnetic-interfaces. This report discussed some 2D ferromagnets and graphene-based materials with considerable value of spin-polarization for efficient spin transmission and dynamic control through exotic heterostructures [35].

Therefore, comparison of these reports with other studies is not appropriate. The study reported by Zhou et al and co-workers shows that graphene-passivated cobalt as a spin-polarized electrode with positive spin polarization properties [36].

3.4. Gate controlled magnetoresistance

Fig. 7(a–f) shows the series of MR variation with gate voltage ranging from −0.5 V to 2 V for Top-Gated s-FET. The results reveal that by increasing gate voltage the magnetoresistance monotonically reduces. This trend indicates that MR can be controlled by gate voltage. The decrease in MR by increasing gate voltage ascribed to the localized trap states in the interlayers [37].

Similarly, the Fig. 8(a–f) shows the series of MR variation with gate voltage ranging from −0.5 V to 2 V for Back-Gated s-FET. Here also, the amplitude of MR decreases with increasing value of gate voltage. In the case of both devices, around the gate voltage value of 2 V, amplitude of MR disappears and MR curve shows noisy behavior. At the large

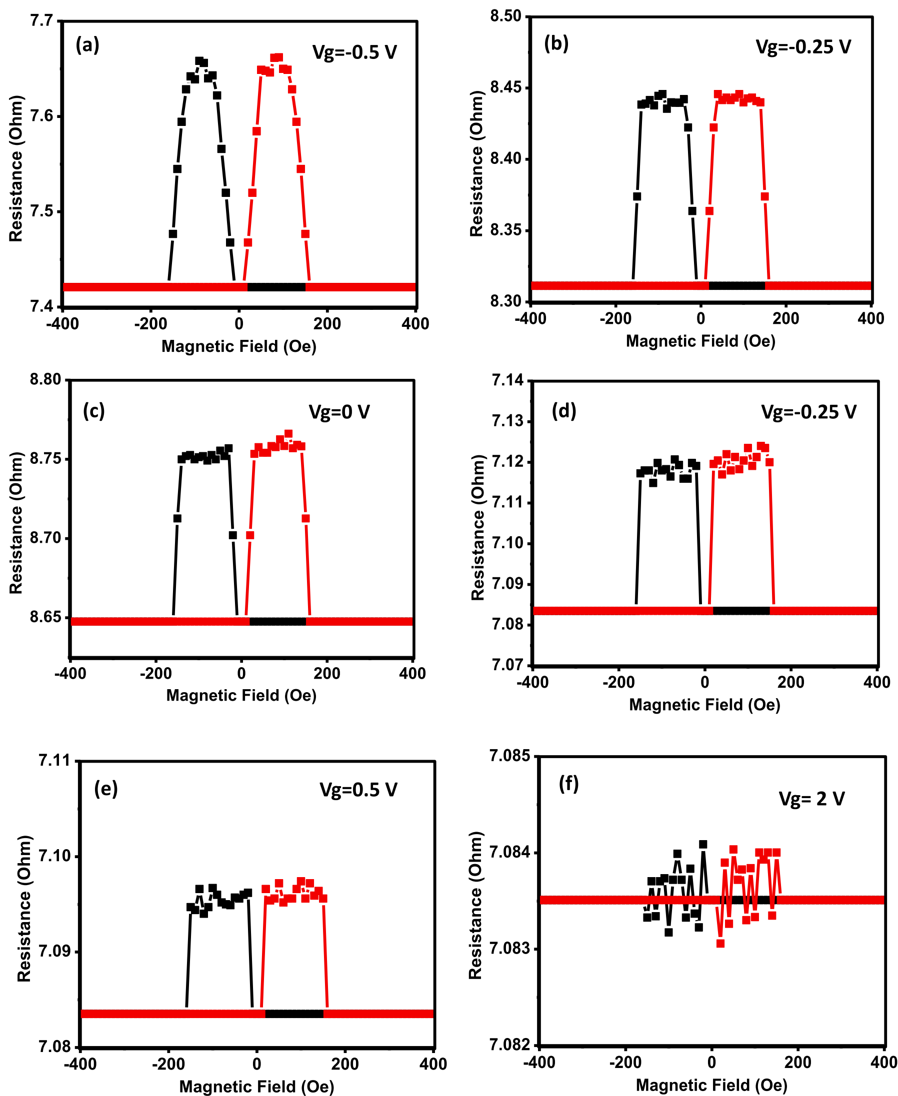

Fig. 8. Gate-controlled MR measurements in Back-Gated s-FET at gate voltage (a) −0.5 V, (b) 0.25 V, (c) 0 V, (d) 0.25 V, (e) 0.5 V and (f) 2 V at room temperature 298 K.

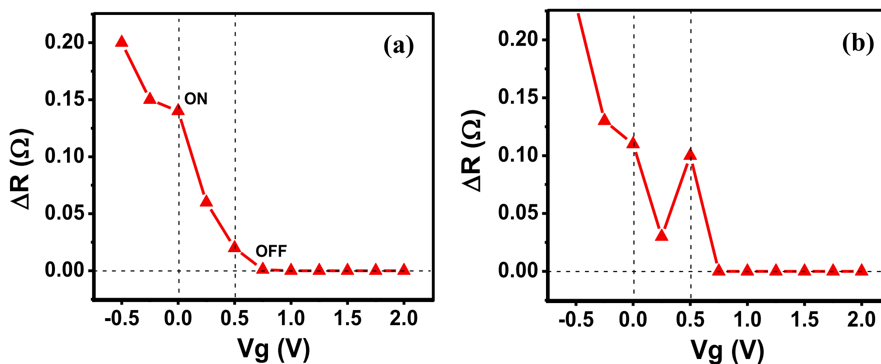

Fig. 9. Switching (ON/OFF state) of (a) Top-Gated s-FET and (b) Back-Gated s-FET based on ΔR of MR curve at room temperature 298 K.

value of gate voltage, the spin excitations localized at the interfaces between FM electrodes. Unfortunately, we did not understand the reason behind flat nature of the parallel state of the magnetization.

3.5. Switching of s-FETs

Finally, we investigated the switching action in Top-Gated s-FET (Fig. 9(a)) and Back-Gated s-FET (Fig. 9(b)) based on amplitude modulation of MR curve at room temperature 298 K. Here, the switching action in both the devices is presented in the form of amplitude

modulation of MR curve (Amplitude of MR curve |ΔR = Rap − Rp|). Through this approach, we successfully archive switching action in Top-Gated s-FET in the gate voltage range −0.5 to 2 V, but unfortunately, appropriate switching action for Back-Gated Type s-FET is not witnessed. To maintain the reproducibility of results, the value of ΔR used in this study is the average of five sets of results.

The considerable variation and vanishing MR by the application of gate voltage operates devices from ON to OFF state, indicates that CGNs based ferromagnetic electrodes have an efficient electrical spin-control operation at room temperature. This spin-control operation at room temperature using gate voltage is attributed to efficient variation of magnetoresistance in the semiconductor channel due to the on/off state of the channel. This is the indication of healthier spin transport [38].

In our case, Top-Gated s-FET and Back-Gated s-FET shows different sets of MR data for same temperature values. In filed effect transistors, contact resistance and mobility in transistors is sensitive to gate voltage and operating temperature. Urban et al demonstrated that increasing the temperature lowers the carrier mobility and exhibits considerable influence on the contact resistance as a function of applied gate voltage [39]. Therefore, device with different architecture behaves differently. In our case, it may be due to the modifications in the graphene density of states due to the coupling of graphene to Co d-states, which results in formation of electron-hole puddles [40,41].

4. Conclusions

In conclusion, we have demonstrated Top-Gated s-FET and Back-Gated s-FET with CGNs based ferromagnetic electrodes. The ohmic contact study of both the devices that is Top-Gated s-FET and Back-Gated s-FET shows that the contacts between CGNs based ferromagnetic electrodes and 2-dimensional electron gas are Ohmic in nature. Similarly, the electrical resistance increases with increasing temperature, which indicates that 2-dimensional electron gas behaves like metal.

The MR study at different temperature reveals that MR decreases monotonically by increasing the temperature for both devices. The highest value of MR was obtained at 50 K, for both devices. This higher value of MR ascribed to the greater value of spin-polarization found in CGNs based ferromagnetic electrodes at lower temperature. The main accomplishment of present work is that the MR of both devices shows good dependence on gate voltage. In addition to this, switching action found appropriate for Top-Gated s-FET. These results motivate and provide a possible avenue for future spintronics applications such as magnetic memory, spin-oscillators and logic devices.

Declaration of Competing Interest

The authors declare that they not have conflict of interest in term financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The raw/processed data required to reproduce these findings cannot be shared at this time as the data also forms part of an ongoing study.

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